TS128MSD64V3A

200PIN DDR333 Unbuffered SO-DIMM
1GB With 64Mx8 CL2.5

Description

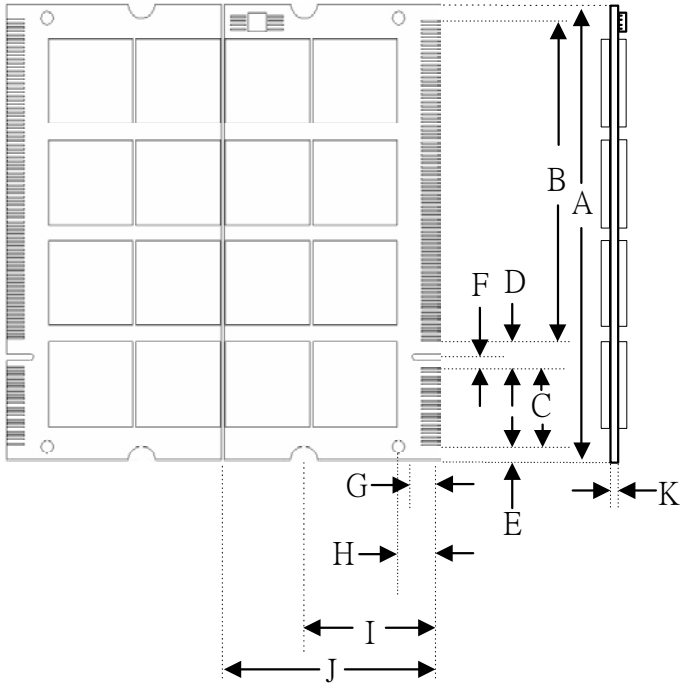
The TS128MSD64V3A is a 128M x 64bits Double Data Rate SDRAM high-density for DDR333. The TS128MSD64V3A consists of 16pcs CMOS 64Mx8 bits Double Data Rate SDRAMs in 60 Ball FBGA packages and a 2048 bits serial EEPROM on a 200-pin printed circuit board. The TS128MSD64V3A is a Dual In-Line Memory Module and is intended for mounting into 200-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Power supply: VDD= VDDQ: 2.5V ± 0.1V,
- Max clock Freq: 166MHZ.
- Double-data-rate architecture; two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CLK transition
- Commands entered on each positive CLK edge
- Auto and Self Refresh.
- Data I/O transactions on both edge of data strobe.
- Serial Presence Detect (SPD) with serial EEPROM
- SSTL-2 compatible inputs and outputs.
- MRS cycle with address key programs.
  CAS Latency (Access from column address) : 2.5
  Burst Length (2,4,8)
  Data Sequence (Sequential & Interleave)

Placement



PCB: 09-1870

Dimensions

Side	Millimeters	Inches
A	67.60±0.20	2.661±0.008
B	47.40	1.866
C	11.40	0.449
D	4.20	0.165
E	2.15	0.085
F	1.80	0.071
G	4.00	0.157
H	6.00	0.236
I	20.00	0.787
J	31.75±0.20	1.250±0.008
K	1.00±0.10	0.039±0.004

(Refer Placement)

Pin Identification

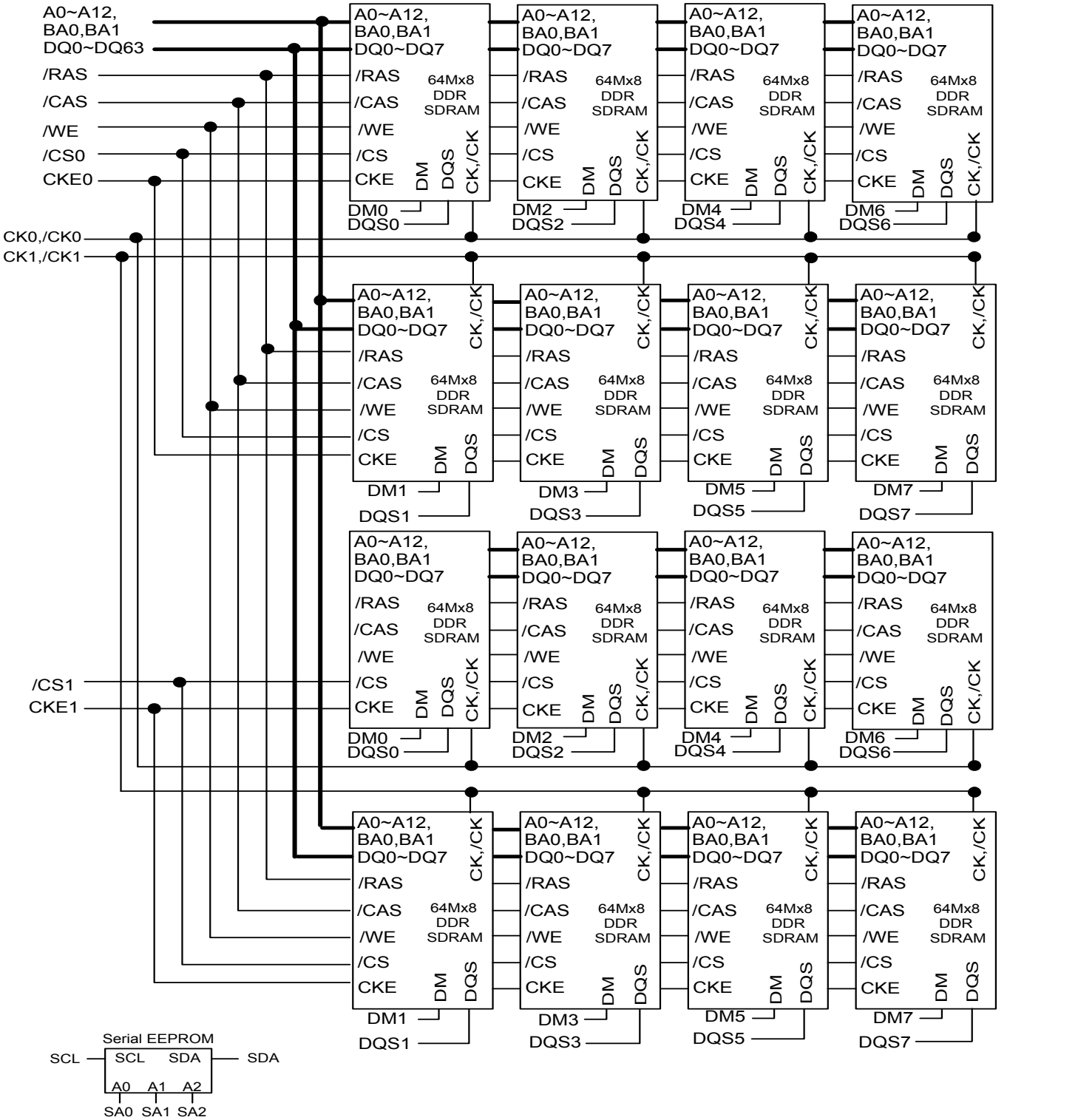
Symbol	Function
A0~A12, BA0, BA1	Address input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobe input/output
CK0~CK2 /CK0~/CK2	Clock Input.
CKE0, CKE1	Clock Enable Input.
/CS0, /CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data-in Mask
VDD	+2.5 Voltage power supply
VREF	Power Supply for Reference
VDDSPD	+2.5 Voltage Serial EEPROM Power Supply
SA0~SA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	69	VDD	137	VSS	02	VREF	70	VDD	138	VSS
03	VSS	71	*CB0	139	DQ35	04	VSS	72	*CB4	140	DQ39
05	DQ0	73	*CB1	141	DQ40	06	DQ4	74	*CB5	142	DQ44
07	DQ1	75	VSS	143	VDD	08	DQ5	76	VSS	144	VDD
09	VDD	77	*DQS8	145	DQ41	10	VDD	78	*DM8	146	DQ45
11	DQS0	79	*CB2	147	DQS5	12	DM0	80	*CB6	148	DM5
13	DQ2	81	VDD	149	VSS	14	DQ6	82	VDD	150	VSS
15	VSS	83	*CB3	151	DQ42	16	VSS	84	*CB7	152	DQ46
17	DQ3	85	DU	153	DQ43	18	DQ7	86	DU	154	DQ47
19	DQ8	87	VSS	155	VDD	20	DQ12	88	VSS	156	VDD
21	VDD	89	*CK2	157	VDD	22	VDD	90	VSS	158	/CK1
23	DQ9	91	*/CK2	159	VSS	24	DQ13	92	VDD	160	CK1
25	DQS1	93	VDD	161	VSS	26	DM1	94	VDD	162	VSS
27	VSS	95	*CKE1	163	DQ48	28	VSS	96	CKE0	164	DQ52
29	DQ10	97	*A13	165	DQ49	30	DQ14	98	DU	166	DQ53
31	DQ11	99	*A12	167	VDD	32	DQ15	100	A11	168	VDD
33	VDD	101	A9	169	DQS6	34	VDD	102	A8	170	DM6
35	CK0	103	VSS	171	DQ50	36	VDD	104	VSS	172	DQ54
37	/CK0	105	A7	173	VSS	38	VSS	106	A6	174	VSS
39	VSS	107	A5	175	DQ51	40	VSS	108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61
47	DQS2	115	A10	183	DQS7	48	DM2	116	BA1	184	DM7
49	DQ18	117	BA0	185	VSS	50	DQ22	118	/RAS	186	VSS
51	VSS	119	/WE	187	DQ58	52	VSS	120	/CAS	188	DQ62
53	DQ19	121	/CS0	189	DQ59	54	DQ23	122	*/CS1	190	DQ63
55	DQ24	123	DU	191	VDD	56	DQ28	124	DU	192	VDD
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2
63	VSS	131	VDD	199	VDD	64	VSS	132	VDD	200	DU
65	DQ26	133	DQS4			66	DQ30	134	DM4		
67	DQ27	135	DQ34			68	DQ31	136	DQ38		

* Please refer Block Diagram

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on V_{DD} supply to Vss	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min		Unit	Note
Supply voltage	VDD	2.4	2.6	V	
I/O Supply voltage	VDDQ	2.4	2.6	V	
I/O Reference voltage	VREF	V_{DDQ}/2-50mV	V_{DDQ}/2+50mV	V	1
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	VIH(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	VIL(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and /CK inputs	VIN(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and /CK inputs	VID(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and /CK inputs	VIX(DC)	1.15	1.35	V	5
Input leakage current	I_I	-10	10	uA	
Output leakage current	I_{OZ}	-10	10	uA	
Output High Current (Normal strength driver) VOUT= 1.95	I_{OH}	-16.8		mA	
Output Low Current (Normal strength driver) VOUT= 0.35	I_{OL}	16.8		mA	
Output High Current (Half strength driver) VOUT= VTT + 0.45V	I_{OH}	-9		mA	
Output High Current (Half strength driver) VOUT= VTT - 0.45V	I_{OL}	9		mA	

1. Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled. TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of <=3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF

the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.

level of the same.

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted,VDD=2.7V TA = 10°C)

Parameter	Symbol	Max.	Unit	Note
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK= tCK min DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	IDD0	1466	mA	
Operating current - One bank Active-Read-Precharge; Burst=2; tRC=tRC min; CL=2.5; tCK=tCK min; VIN=VREF fro DQ,DQS and DM	IDD1	1625	mA	
Percharge power-down standby current; All banks idle; power –down mode; CKE = <VIL(max); tCK= tCK min VIN = VREF for DQ,DQS and DM	IDD2P	165	mA	
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); tCK=166Mhz for DDR333 Address and other control inputs changing once per clock cycle; VIN = VREF for DQ,DQS and DM	IDD2F	533	mA	
Active power - down standby current ; one bank active; power-down mode; CKE<= VIL (max); tCK = tCK min; VIN = VREF for DQ,DQS and DM	IDD3P	214	mA	
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK = tCK min; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	765	mA	
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; CL=2.5 at tCK = tCK min ; 50% of data changing at every burst; lout = 0 mA	IDD4R	1,840	mA	
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2.5 at tCK = tCK min ; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W	1,720	mA	
Auto refresh current; tRC = tRFC(min)	IDD5	3,429	mA	
Self refresh current; CKE <= 0.2V;	IDD6	64	mA	
Operating current - Four bank operation; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7	3,774	mA	

1. Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading capacitor.

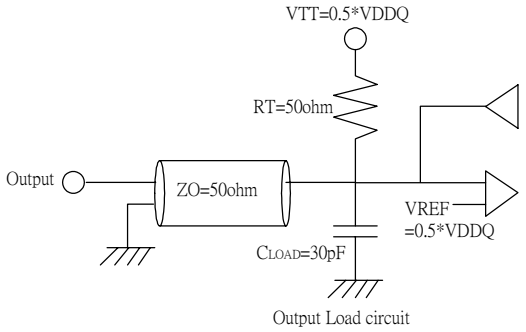
AC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V	2

Note:
1. VIH(max)=4.2V. The overshoot voltage duration is <=3ns at VDD.
2. VIL(min)=-1.5V. The undershoot voltage duration is <=3ns at VSS
3. VID is the magnitude of the difference between the input level on CK and the input on /CK
4. The Value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (VDD=2.5, VDDQ=2.5, TA=0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5*VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels (VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	VTT	V	
Output load condition	See Load Circuit		



Output Load circuit

Input/Output CAPACITANCE (VDD = 2.5V, VDDQ = 2.5V,TA = 25°C, f = 1MHz)

Parameter	Symbol		Max	Unit
Input capacitance (A0~A12, BA0~BA1, /RAS, /CAS, /WE)	CIN1	34	56	pF
Input capacitance (CKE0,CKE1)	CIN2	18	26	pF
Input capacitance (/CS0,/CS1)	CIN3	18	26	pF
Input capacitance (CK0, CK1)	CIN4	18	26	pF
Input capacitance (DM0~DM7)	CIN5	10	12	pF
Data and DQS input/output capacitance (DQ0~DQ63)	COUT1	10	12	pF

AC Timing Parameters & Specifications

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
Row cycle time	tRC	60		ns	
Refresh row cycle time	tRFC	72		ns	
Row active time	tRAS	42	120K	ns	
/RAS to /CAS delay	tRCD	18		ns	
Row active to Row active delay	tRP	18		ns	
Row active to Row active delay	tRRD	12		ns	
Write recovery time	tWR	15		tCK	
Last data in to Read command	tCDLR	1		tCK	
Col. Address to Col. Address delay	tCCD	1		tCK	
Clock cycle time	tCK	6	12	ns	4
Clock high level width	tCH	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	tCK	
DQS-out access time from CK /CK	tDQSCK	-0.70	0.75	ns	
Output data access time from CK /CK	tAC	-0.70	0.75	ns	
Data strobe edge to output data edge	tDQSQ		0.45	ns	4
Read Preamble	tRPRE	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.75	1.25	tCK	
DQS-in setup time	tWPRES	0		ns	2
DQS-in hold time	tWPREH	0.25		tCK	
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK	
DQS-in high level width	tDQSH	0.35		tCK	
DQS-in low level width	tDQSL	0.35		tCK	
DQS-in cycle time	tDSC	0.9	1.1	tCK	
Address and Control input setup time	tIS	0.75		ns	
Address and Control input hold time	tIH	0.75		ns	
Data-out high-impedance time from CK, /CK	tHZ	-0.70	+0.70	ns	
Data-out low-impedance time from CK, /CK	tLZ	-0.70	+0.70	ns	
Mode register set cycle time	tMRD	2		tck	
DQ & DM setup time to DQS	tDS	0.45		ns	

DQ & DM hold time to DQS	tDH	0.45		ns	
DQ & DM input pulse width	tDIPW	1.75		ns	
Power down exit time	tPDEX	6		ns	
Exit self refresh to bank active command	tXSA	7.5		ns	5
Exit self refresh to read command	tXSR	200		Cycle	
Refresh interval time	tREF	7.8		us	1
Clock half period	tHP	tCLmin or tCHmin		ns	
Data hold skew factor	tQHS		0.55	ns	
DQS write post amble time	tWPST	0.4	0.6	tck	3

Note:

2. The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The Maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are >= 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
5. A write command can be applied with tRCD satisfied after this command.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	$BA_{0,1}$	A_{10}/AP	A_0~A_9,A_{11}, A_{12}	Note
Register	Extended Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry		H	L	H	X	X	X	X			
					L	V	V	V				
	Exit		L	H	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X			
					L	H	H	H				
	Exit		L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No Operation Command			H	X	H	X	X	X	X			9
					L	H	H	H				9

1. OP Code: Operand Code. A0 ~ A12 & BA0 ~ BA1: Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM. The automatically precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.

   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

   after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in is masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	DDR SDRAM	07
3	# of Row Addresses on this Assembly	13	0D
4	# of Column Addresses on this Assembly	11	0B
5	# of Module Rows on this Assembly	2bank	02
6	Data Width of this Assembly	64bits	40
7	Data Width of this Assembly	0	00
8	VDDQ and Interface Standard of this Assembly	SSTL-2	04
9	DDR SDRAM Cycle Time at CAS Latency=2.5	6ns	60
10	DDR SDRAM Access Time from Clock at CL=2.5	±0.70ns	70
11	DIMM configuration type (non-parity, Parity, ECC)	NON-ECC	00
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary DDR SDRAM Width	X8	08
14	Error Checking DDR SDRAM Width	-	00
15	Min Clock Delay for Back to Back Random Column Address	tCCD=1CLK	01
16	Burst Lengths Supported	2,4,8	0E
17	# of banks on each DDR SDRAM device	4 bank	04
18	CAS Latency supported	2.5 , 2	0C
19	CS Latency	0 CLK	01
20	WE Latency	1 CLK	02
21	DDR SDRAM Module Attributes	Differential Clock Input	20
22	DDR SDRAM Device Attributes: General	Fast / current AP	00
23	DDR SDRAM Cycle Time CL=2.0	7.5ns	75
24	DDR SDRAM Access from Clock CL=2.0	±0.70ns	70
25	DDR SDRAM Cycle Time CL=1.5	-	00
26	DDR SDRAM Access from Clock CL=1.5	-	00
27	Minimum Row Precharge Time (tRP)	18ns	48
28	Minimum Row Active to Row Activate delay (tRRD)	12ns	30
29	Minimum RAS to CAS Delay (tRCD)	18ns	48
30	Minimum active to Precharge time (tRAS)	42ns	2A
31	Module ROW density	512MB	80
32	Command/Address Input Setup Time	0.75ns	75
33	Command/Address Input Hold Time	0.75ns	75
34	Data Signal Input Setup Time	0.45ns	45
35	Data Signal Input Hold Time	0.45ns	45
36-40	Superset Information	-	00
41	DDR SDRAM Minimum Active / Auto Refresh Time(tRC)	-	00

42	DDR SDRAM Minimum Auto-Refresh to Active / Auto Refresh Command Period(tRFC)	-	00					
43	DDR SDRAM Maximum Device Cycle Time(tCK max)	-	00					
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	-	00					
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	-	00					
46	PLL Relock Time	-	00					
47-61	Superset Information	-	00					
62	SPD Data Revision Code	-	00					
63	Checksum for Bytes 0-62	-	7D					
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS128MSD64V3A	54	53	31	32	38	4D
			53	44	36	34	56	33
			41	00	00	00	00	00
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Unused Storage Locations	Undefined	-					